Abstract for an Invited Paper

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Polyphase Filters, Distribution-Based Noise Estimators, and Other Techniques for Wideband SETI*

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The NASA High Resolution Microwave Survey (HRMS) Sky Survey will observe a simultaneous dual-polarization bandpass of over 300 MHz as it searches for continuous-wave (CW) signals over the 1 GHz to 10 GHz frequency range. The high data throughput rates and signal processing speed required to observe the wide instantaneous bandpass require efficient algorithms and hardware impIementations. This paper will discuss the algorithms and hardware planned for the operational system. This includes a comparison of the sensitivity of a matched falter detection system for CW signal sources passing through the antenna beam response to the sensitivities of a windowed Discrete Fourier Transform (DFT) system and a polyphase-DFT system. The polyphase-DFT system is shown to approximate closely an ideal bandpass filter bank with a small amount of processing in addition to the DFT, improving the sensitivity by almost 3 dB over a windowed DFT system. Sidelobe rejection of the polyphase-DFT system is superior to windowed DFTs. This enhanced sidelobe rejection will help to isolate spectrally the effects of radio frequency interference (RFI) in these wideband observations. The presence of RFI in the wideband input also challenges real-time dynamic noise power estimation, required for constant false alarm rate signal detection. The noise power is estimated using order statistics to sample the probability distribution function. Ordinarily, obtaining order statistics would require real-time sorting or histogramming of the input data stream. The high data throughput for the HRMS Sky Survey makes this impractical. However, by limiting the dynamic range within which the noise power is to be estimated, simple 1/0 efficient techniques based on a priori estimates can be used. High throughput also prohibits the system from taking advantage of high-density DRAM memories for reordering of the multimegapoint data array. By visualizing data orderings as vectors of address bits, more efficient data orderings can be designed. The resulting rearrangement in address patterns allows double-buffer memory banks to be reduced to single-buffer banks, reducing the necessary hardware.

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